ABSTRACT

A memory device includes a memory array of thin film transistor (TFT) memory cells. The memory cells include a floating gate separated from a gate electrode portion of a gate line by an insulator. The gate electrode portion includes a diffusive conductor that diffuses through the insulator under the application of a write voltage. The diffusive conductor forms a conductive path through the insulator that couples the gate line to the floating gate, changing the gate capacitance and therefore the state of the memory cell. The states of the memory cells are detectable as the differing current values for the memory cells. The memory cells are three terminal devices, and read currents do not pass through the conductive paths in the memory cells during read operations. This renders the memory cells robust, because read currents will not interfere with the storage mechanism in the memory cells. The memory array can be fabricated using multiple steps using the same mask. The use of a single mask for multiple steps reduces the time and cost involved in fabricating the memory array.